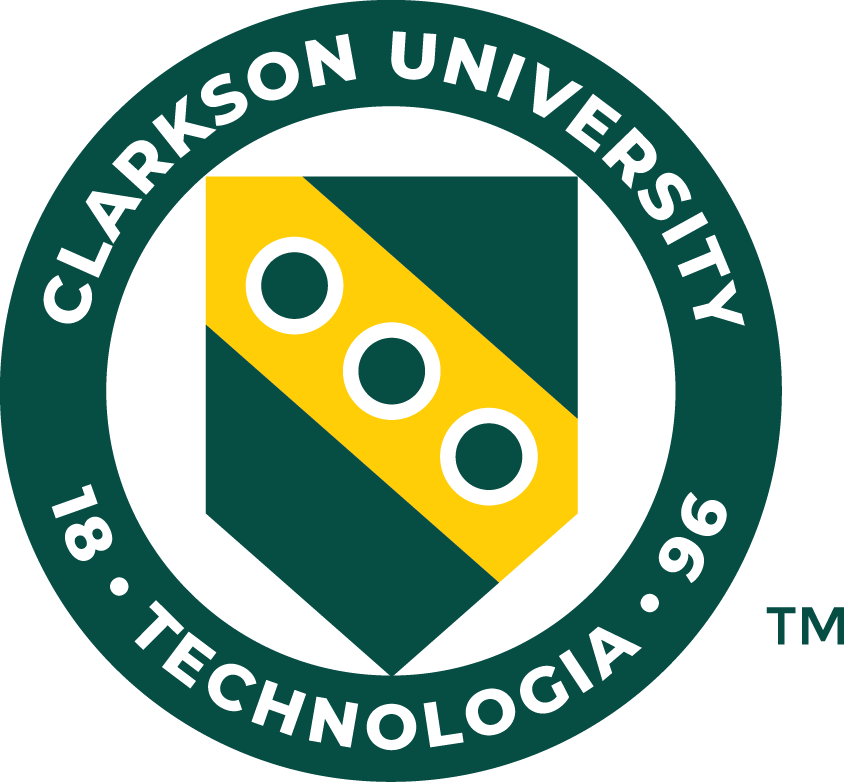
EE 316 Computer Engineering Junior Lab

Design Project 3

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**Summary:**

The project involves the design and implementation of a comprehensive analog waveform sampling and reconstruction system using the Trenz ZynqBerry board with GPIO Pins and various components, including a function generator, I2C LCD display, PCF8591 ADC-DAC module, op-amp adder circuit, and PWM output. The op-amp adder ensures a peak-to-peak amplitude of 3.3 Volts for periodic sinusoidal waveforms generated by the function generator, while the PCF8591 ADC-DAC module facilitates accurate analog signal sampling from multiple sensors. The PWM output, controlled by user-selected inputs, undergoes reconstruction through a low-pass filter. The system also generates a clock output whose frequency is modulated by a potentiometer, thermistor, and LDR. An I2C LCD display provides real-time information about the selected source for the PWM signal and indicates the system's current clock generation status. The overarching objectives include maximizing the bandwidth of sampled analog signals without aliasing and minimizing errors for precise frequency reconstruction. This integrated system offers a versatile solution for waveform analysis and display.

**Problem Decomposition:**

The project has been strategically segmented into five distinct groups, each assigned a specific set of tasks crucial to the overall functionality of the system.

Group 1 - PCF8591 ADC-DAC Interfacing with I2C:

This group is primarily dedicated to the seamless integration of the PCF8591 ADC-DAC module with the I2C protocol. It is imperative to adhere to specific parameters, including a maximum sampling frequency capped at 11.1KHz and an I2C maximum bus speed locked at 100KHz. The custom I2C address configuration involves setting "1001000" when all A2, A1, and A0 are set to 0. The input to this module comprises an analog signal, meticulously created with a DC offset and a precise peak-to-peak amplitude of 3.3 volts. The desired output from this module is a digital signal.

Group 2 - LCD:

The second group undertakes the responsibility of interfacing with the LCD. Noteworthy specifications include a default I2C address of "0100111" and the utilization of a 4-bit data configuration to accommodate the I2C's maximum 8-bit data per transaction. The sequence of data transmission involves sending bits D7 to D4 first, followed by D3 to D0.

Group 3 - PWM:

Group 3 focuses on the Pulse Width Modulation (PWM) aspect of the system. Their tasks involve reading an 8-bit value from the I2C, with the PWM signal's duty cycle intricately tied to this 8-bit data. Users are granted the flexibility to choose between four inputs for PWM determination, facilitated through a button interface. The AIN2 input undergoes processing through a Low Pass Filter (LPF) before being directed to the oscilloscope for visualization.

Group 4 - Clock Generation:

The fourth group takes charge of the critical task of clock generation within the system. The clock output exhibits a variable frequency, oscillating between 500 and 1500 Hz. This frequency modulation is contingent on the values of ADR, offering dynamic adjustments. The clock generation module's activation or deactivation is tied to a specific button press, denoted as btn1.

Group 5 - Op-Amp Adder Circuit:

The final group concentrates on the Op-Amp adder circuit, designed to ensure that periodic sinusoidal waveforms, generated by an external function generator, conform to a specified peak-to-peak amplitude of 3.3 volts. This is achieved by adding the input signal to 3.3 volts through an op-amp adder configured with a gain of 1/2.

By distributing the project into these five groups, each equipped with a well-defined set of objectives, the project team can efficiently navigate through the intricacies of the design, fostering a systematic and collaborative approach to achieving the overarching goals of analog waveform sampling and reconstruction.

**Detailed Design and Module level Testing (Design for Testing)**

The designed system aims to sample, store, display, and recreate analog waveforms using the Trenz ZynqBerry board with GPIO Expansion board, a function generator, a 16x2 character I2C LCD display module, a PCF8591 ADC-DAC module with I2C interface, and additional components such as Op-Amps, capacitors, and resistors.

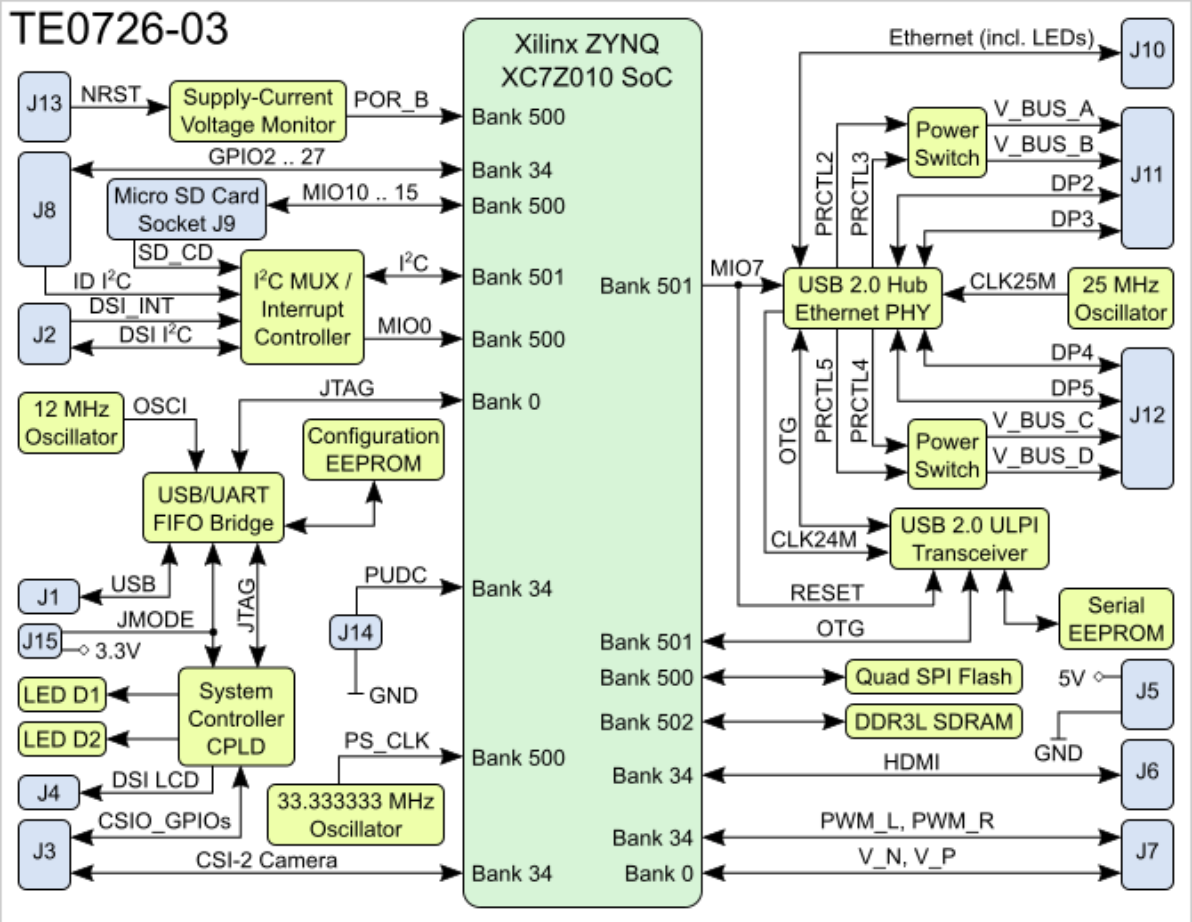


Figure: block diagram of Trenz Electronic TE0726

Op-Amp Adder Circuit:

Periodic sinusoidal waveforms, generated by the function generator, with a peak-to-peak amplitude of 3.3 Volts are used as input. Since the PCF8591 ADC requires positive analog voltages, an Op-Amp adder circuit is employed to add 3.3 volts to the input signal with a gain of 1/2.

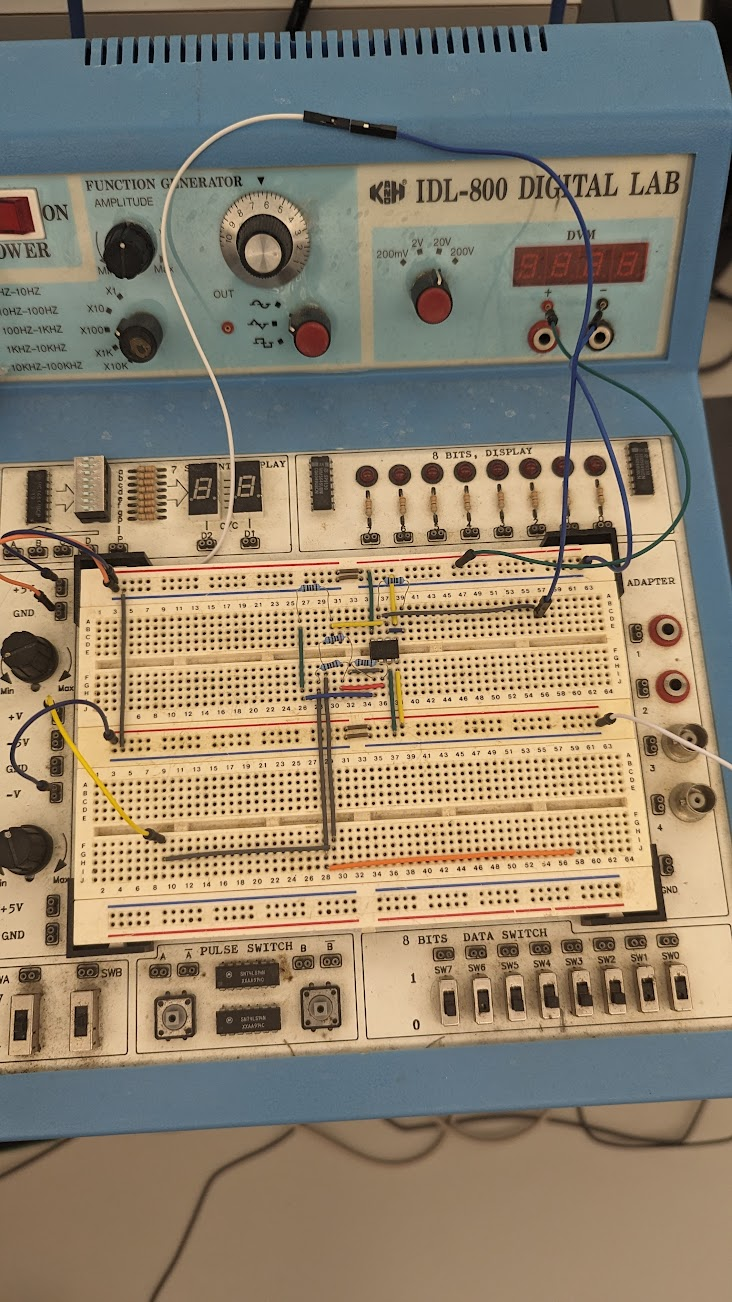


Figure: Picture of Op-Amp adder circuit.

ADC:

The PCF8591 module, featuring 4 input channels (AIN0 to AIN3), interfaces with various sensors through jumpers. The ANALOG\_INPUT from the Op-Amp circuit connects to AIN2. The other three inputs, AIN0, AIN1, and AIN3, are linked to sensors: Light Dependent Resistor (LDR), Thermistor (TEMP), and Potentiometer (POT) respectively.

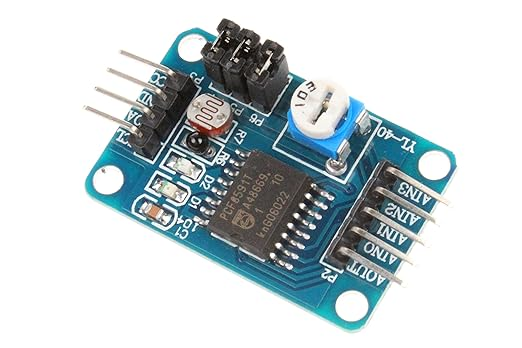


Figure: Picture of ADC module

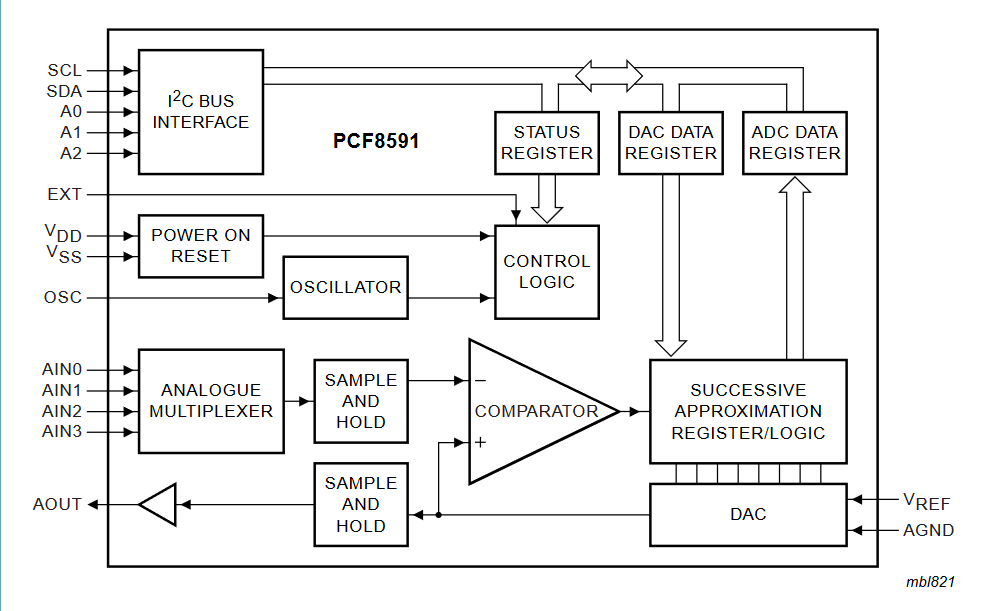
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Figure: Block Diagram for PCF8591

PWM:

The system incorporates PWM output, and the duty cycle is determined by the 8-bit value of the data. Users can select between the four inputs using the PMOD button (BTN1) to set the PWM duty cycle. The PWM output undergoes low-pass filtering to reconstruct input signals for display on an oscilloscope. For AIN2 input, a sinusoidal waveform is displayed on the oscilloscope alongside the original input. The system's capability to reconstruct input signals is limited by the highest input frequency.

Clock Generation:

The system generates a clock output with a variable frequency between 500 to 1500 Hz, controlled by the Potentiometer, Thermistor, and LDR. The clock generation module can be enabled or disabled using BTN2, with PMOD LEDs indicating its states.

LCD:

An I2C LCD is connected to the Zynq board, displaying information about the selected source for the PWM signal on the first line (LDR, TEMP, or POT). The second line indicates whether the system is currently generating a clock output.

Reset functionality is implemented using the PMOD button BTN0. The project is developed using Vivado 2019.1, leveraging the board files already installed on AppsAnywhere. This system offers a comprehensive solution for analog waveform manipulation and visualization, incorporating various sensors, PWM generation, clock generation, and LCD display for user interaction and system monitoring.

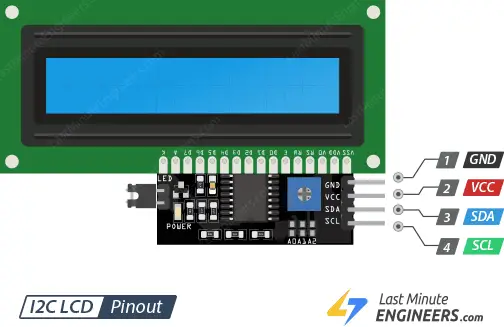
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Figure: Pinout of LCD with PCF8591 adapter to I2C

The inputs for the I2C Bus Interface A2 are connected to the output of our filters output which then outputs an 8-bit number sent to two locations: our PWM generator and Our clock Generator.

The PCF8591 can be accessed and configured through the I2C bus interface. To interact with the PCF8591, you would typically send commands to its address on the I2C bus, followed by the data you want to write to its registers or request a read from them. For instance, you can enable or disable the analog output, select the input channel for the ADC, and configure the input mode (single-ended or differential)

**Alternative Designs:**

Our team opted for a single I2C bus. Going with a single bus offers simplicity in hardware design and reduced system complexity. This approach is often preferred when dealing with constraints such as limited I/O pins, as it lowers the overall required pin count from the board. Additionally, a shared communication medium allows devices to communicate directly with each other, simplifying interactions. However, challenges may arise, such as the potential for address conflicts among devices on the same bus, limiting overall bandwidth, and introducing distance limitations due to signal integrity concerns.

On the other hand, employing two I2C buses provides several benefits. It allows for address isolation, mitigating the risk of conflicts by assigning unique addresses to devices on separate buses. This can be particularly advantageous in large systems with numerous devices. Improved bandwidth is another advantage, as devices on separate buses can communicate concurrently, potentially enhancing overall system performance. Additionally, the flexibility of system expansion is increased, as new devices can be added to a separate bus without affecting the existing one. However, this approach introduces higher complexity in hardware design, a higher pin count, and the potential for redundancy if devices on different buses need to communicate directly.

Ultimately, the choice between one or two I2C buses depends on the requirements, taking into consideration factors such as the number of devices, address conflicts, bandwidth needs, and hardware constraints.

**Specification Testing:**

Ensuring the proper functionality of the PWM entity requires a multi-step process. We begin with basic functionality tests, applying a clock signal and verifying the PWM output responds as expected. Different values for `datain` should be tested to confirm the PWM signal aligns with the counter value. Additionally, the behavior of the `PWMState` variable during transitions needs to be checked, ensuring the counter resets correctly.

Next, we explored edge cases by testing with the maximum and minimum values for both `N` and `PWMState`. The impact of asserting the `BigReset` signal needs to be verified. To assess the design's robustness under various operating conditions, stress tests are conducted with diverse input combinations, paying close attention to potential overflow issues.

Finally, performance testing is conducted by varying clock frequencies and ensuring the PWM output adapts accordingly on the board.

Testing our clock generation module was a critical phase in ensuring it adherened to specific requirements and reliable operation within your system. We used the simulation tools ModelSim to validate our VHDL code. Design comprehensive testbench scenarios covering various input conditions, including Adjustvar, potentiometer, thermistor, and LDR variations. Which we tested as one case, because they were all returning the same length and type values. Investigate edge cases such as minimum and maximum values to confirm the module's resilience and accuracy.Then tested the clock gen with hardware on the Trenz ZynqBerry board, using oscilloscopes to measure and confirm clock frequency output.

Ensure integration testing within the larger system design, validating proper interactions with other modules like LCD display and PWM generation. Functional verification should confirm the correct representation of the selected PWM source on the LCD and the accurate indication of clock output status. Additionally, evaluate performance by assessing the system's response time to changing input conditions and its ability to generate stable clock signals across differnat scenarios.

**Results and Analysis**

The project achieved the successful design and implementation of a comprehensive analog waveform sampling and reconstruction system using the Trenz ZynqBerry board. The system was organized into five distinct groups, each assigned specific tasks crucial to its overall functionality.

In Group 1, dedicated to PCF8591 ADC-DAC interfacing with I2C, seamless integration with the I2C protocol was achieved, meeting parameters such as a maximum sampling frequency of 11.1KHz and an I2C bus speed of 100KHz. The custom I2C address configuration and Op-Amp adder circuit ensured accurate analog signal sampling from various sensors with a peak-to-peak amplitude of 3.3 Volts.

Group 2 successfully handled the LCD interfacing, integrating the 16x2 character I2C LCD display module. Real-time information about the selected PWM signal source and the system's clock generation status was displayed on the LCD. The reset functionality using the PMOD button BTN0 was implemented effectively.

In Group 3, focusing on PWM generation, the team achieved reading an 8-bit value from the I2C and tying the PWM signal's duty cycle to this data. Users could choose between four inputs for PWM determination through a button interface. The AIN2 input underwent processing through a Low Pass Filter (LPF) before being directed to the oscilloscope for visualization, demonstrating successful signal reconstruction.

Group 4 successfully implemented the clock generation module, producing a variable-frequency output oscillating between 500 and 1500 Hz. The frequency modulation was controlled by inputs from the Potentiometer, Thermistor, and LDR. Activation or deactivation of the clock generation module was tied to a specific button press (btn1), with PMOD LEDs indicating its states.

In Group 5, the Op-Amp adder circuit was designed to ensure periodic sinusoidal waveforms conformed to the specified peak-to-peak amplitude of 3.3 Volts. The gain of 1/2 in the op-amp adder contributed to achieving the desired output.

Alternative Designs were considered, and the team opted for a single I2C bus, providing simplicity in hardware design and reduced system complexity. Thorough testing procedures were conducted, including basic functionality tests, edge case scenarios, stress tests, and performance testing. The results indicated the system's robust performance under diverse operating conditions, meeting specific requirements and adapting to changing input conditions.

In conclusion, the integrated analog waveform sampling and reconstruction system exhibited successful functionality, reliability, and versatility. The strategic division into five groups contributed to the project's overall success in waveform analysis and display.

**References**

* [**https://lastminuteengineers.com/i2c-lcd-arduino-tutorial/**](https://lastminuteengineers.com/i2c-lcd-arduino-tutorial/)
* [**https://www.ti.com/lit/ds/symlink/pcf8574a.pdf**](https://www.ti.com/lit/ds/symlink/pcf8574a.pdf)
* [**https://elettronicablog.files.wordpress.com/2016/03/sensor\_kit\_v2-0\_for\_b\_150928.pdf**](https://elettronicablog.files.wordpress.com/2016/03/sensor_kit_v2-0_for_b_150928.pdf)

**Board schematic**

[**https://moodle.clarkson.edu/pluginfile.php/165307/mod\_label/intro/SCH-TE0726-03R.pdf**](https://moodle.clarkson.edu/pluginfile.php/165307/mod_label/intro/SCH-TE0726-03R.pdf)

**Code**